EE232 PROJECT REPORT

**(10-BIT RING COUNTER)**

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# DESCRIPTION:

The **10-bit ring counter** is a sequential circuit comprising ten flip-flops connected in a circular configuration. It circulates a single logic 1 across the 10 stages with every clock pulse. Unlike a conventional ring counter, this design includes an **adjustable clock speed** feature, allowing the user to control the speed of the circulating bit.

**Key Features:**

1. **Adjustable Clock Speed**: A clock divider module allows users to set the desired operational speed of the counter.
2. **Initialization**: The counter initializes with a single 1 in the least significant bit while all other bits are 0.
3. **Cyclic Behavior**: After 10 clock cycles, the logic 1 completes a full circle and returns to its initial position.

**PROGRESS OF PROJECT**:

 **Design Phase:**

* Developed the VHDL code for the 10-bit ring counter.
* Implemented the clock divider module for speed adjustment using a configurable SPEED signal.

 **Simulation:**

* Verified the counter’s cyclic operation in ModelSim.
* Simulated varying clock speeds to ensure the counter adapts to the user-specified speed.

 **Hardware Preparation:**

* Synthesized the design using Quartus Prime.
* Assigned FPGA pins for inputs (CLK, RST, SPEED) and outputs (Q[9:0]).

# Status of the project:

#  Write the VHDL code for the 10-bit ring counter

#  Clock divider has been developed and simulated successfully.

#  Initial hardware synthesis and testing on the DE10 Lite FPGA board.

# Challenges Encounter:

 **Clock Division Accuracy**:  
Difficulty ensuring precise and stable divided clock signals for varying speeds. Resolved with a counter-based clock divider verified through simulation.

 **Initialization Issues**:  
Incorrect counter states upon reset. Fixed by implementing an explicit asynchronous reset mechanism.

 **Debugging Bit Circulation**:  
Invalid states observed during early simulations. Corrected with robust clock synchronization and state retention logic.

 **Visualizing Outputs**:  
Fast toggling of LEDs was hard to observe. Used a seven-segment display and slower clock speeds for clarity during testing.

# Conclusion:

# The 10-bit ring counter with adjustable clock speed is a practical design demonstrating sequential logic, modular design with a clock divider, and configurable user input. So far:

1. The design and simulation stages have been completed successfully, demonstrating the counter's cyclic behavior and adjustable speed functionality.
2. Hardware testing is progressing as planned, with no significant challenges identified

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**Credits :**

ChatGpt, Google, ModelSim User Manual, Atharva Bhawsar Bhaiya**.**